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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,348	10/10/2003	Kevin D. Kissell	MIPS.0189-00-US	4702

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EXAMINER	
ZHE, MENG YAO	

ART UNIT	PAPER NUMBER
2109	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

Office Action Summary	**Application No.** 10/684,348	**Applicant(s)** KISSELL, KEVIN D.	
	Examiner MengYao Zhe	**Art Unit** 2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/102003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *See Continuation Sheet*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :6/27/05; 12/12/05; 1/13/06; 7/21/05; 12/16/04; 7/20/04; 10/10/03; 4/18/07; 4/03/07; 3/20/07; 2/09/07; 11/30/06; 11/3/05.

DETAILED ACTION

This is the initial Office action based on the 10/684348 application filed on 10/10/2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15 to 28, 67, 76 to 87 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 15 to 28 and claims 76 to 87, it is unclear as to whether they are claiming for a processor or a method, since both words are used in the preamble.

As per claim 67, it states "the mechanism of claim 56". However, claim 56 claims for a digital storage medium, and not a mechanism. Thus, claim 67 is unclear.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 3 to 14, 29 to 41, 69 to 71, 75, are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 3 to 14, 29 to 41, 69 to 71, lack the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 USC 101. Although physical articles such as the processor is mentioned in the preamble of the claim, the actual body of the claim lacks necessary physical articles. They are clearly not a series of steps or act to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material *per se*.

Claim 75 is rejected because it claims for a signal. Merely claiming non-functional descriptive material, i.e., abstract ideas, stored on a computer-readable medium, in a computer, or on an electromagnetic carrier signal, does not make it statutory. See *Diehr*, 450 U.S. at 185-86, 209 USPQ at 8 (noting that the claims for an algorithm in *Benson* were unpatentable as abstract ideas because "[t]he sole practical application of the algorithm was in connection with the programming of a general purpose computer.").

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 6, 8 to 20, 22 to 34, 36 to 47, 49 to 61, 63 to 81, 83 to 87 are rejected under 35 U.S.C. 102(b) as being anticipated by Dupree et al (Dupree), Patent No. 5,949,994.

As per claims 15, 1, 29, 42, 56, 75, 76, 86, Dupree teaches In a processor enabled to support and execute multiple program threads, a method for rescheduling execution or deallocating itself by a thread *(Column 28, lines 1 to 7)*, **comprising:**

> **(a) issuing an instruction that accesses a portion of a record in a data storage device encoding one or more parameters associated with one or more conditions under which the thread is or is not to be rescheduled; and** *(Column 23, lines 1 to 15, Column 27, lines 45 to 65, Column 30, lines 40 to 65: context corresponds to threads, and the scheduler latch contains information about rescheduling of a thread. The scheduler latch corresponds to the record. It is inherent that an instruction was issued to check the status of scheduler latch.)*
>
> **(b) following the conditions for rescheduling according to the one or more parameters in the portion of the record or deallocating the thread.** *(Column 26, lines 3 to 30, Column 27, lines 45 to 67)*

As per claims 16, 2, 30, 43, 57, Dupree teaches the method of claim 15 wherein the record is in a general purpose register (GPR). *(Column 30, lines 60 to Column 31 lines 60; Moreover a GPR is a data storage)*

As per claims 17, 3, 31, 44, 58, 87, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled. *(Column 27, lines 45 to 52)*

As per claims 18, 4, 32, 45, 59, 77, Dupree teaches the method of claim 17 wherein the parameter associated with the thread being deallocated is a value of zero. *(Fig 4B: no NAND gates. Column 25, lines 10 to 16: setting a bit and the fact that there is no NAND gate in the circuit means asserted high for scheduling. Therefore, zero for deallocation.)*

As per claims 19, 5, 33, 46, 60, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being requeued for scheduling. *(Column 32, lines 40 to 61; Column 25, lines 10 to 16)*

As per claims 20, 6, 34, 47, 61, Dupree teaches the method of claim 19 wherein the parameter is any-odd-value. *(Column 25, lines 10 to 16: the thread to be scheduled must have its scheduling bit set to 1, which is an odd value.)*

As per claims 22, 49, 63, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread relinquishing execution to another thread until a specific condition is met *(Column 26, lines 15 to 30)*

As per claims 23, 9, 50, 64, Dupree teaches the method of claim 22 wherein the parameter is encoded in one of a bit vector or one or more value fields in the record. *(Column 25, lines 10 to 16, Column 31, lines 5 to 60)*

As per claims 24, 10, 51, Dupree teaches the method of claim 15 wherein, in the circumstance of the thread issuing the instruction and being rescheduled, execution of the thread resumes, upon the one or more conditions being met, at a place in the thread instruction stream following the instruction that the thread issued. *(Column 27, lines 45 to 67, Column 32, lines 20 to 60)*

As per claim 25, 38, 52, 65, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled, and another of the parameters is associated with the thread being requeued for scheduling. *(Column 27, lines 45 to 67: the PC is set for interrupt if to be rescheduled, which corresponds to another parameter. The a bit for the thread in the scheduler latch would be unset if the thread is to be deallocated.)*

As per claim 26, 8, 39, 53, 66, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45 to 67: relinquish until condition is met corresponds to rescheduling.)*

As per claim 27, 40, 54, 57, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being requeued for rescheduling, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45 to 67: The two scenarios are equivalent since after the condition is met, the thread must be rescheduled.)*

As per claim 28, 41, 55, 68, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled, another of the parameters is associated with the thread being requeued for scheduling, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45 to 67: The two scenarios are equivalent since after the condition is met, the thread must be rescheduled.)*

As per claim 11, Dupree teaches the mechanism of claim 3 wherein, when the parameter equals a third value, the third value being different from the first and second values, the instruction unconditionally reschedules the program thread. *(Column 23, lines 1 to 5, Column 25, lines 50 to 67, Column 26, lines 15 to 30: there are different states for a context. When it is in the bidding state, the context has been scheduled unconditionally, and has an interrupt pending. Each state is represented by different values.)*

As per claim 12, Dupree teaches the mechanism of claim 1 wherein one of the one or more conditions is a hardware interrupt. *(Column 25, lines 9 to 30)*

As per claim 13, Dupree teaches the mechanism of claim 1 wherein one of the one or more conditions is a software interrupt. *(Column 25, lines 50 to 57)*

As per claim 14, Dupree teaches the mechanism of claim 1 wherein, in the circumstance of the program thread being rescheduled, execution of the program thread resumes at a place in the thread following the instruction. *(Column 27, lines 45 to 67, Column 32, lines 20 to 60)*

As per claim 36, Dupree teaches the digital processor of claim 29 wherein one of the parameters is associated with the thread relinquishing execution to another thread until a specific condition is met. *(Column 25, lines10 to 17, lines 50 to 67; Column 26, lines 3 to 15; Column 27, lines 45 to 67: relinquishing until a condition is met corresponds to interrupt and its service routines followed by rescheduling.)*

As per claim 37, Dupree teaches the digital processor of claim 36 wherein the parameter is encoded in one of a bit vector or one or more value fields in the record. *(Column 25, lines 10 to 20, Column 27, lines 45 to 67: latch and registers all corresponds to bit vector.)*

As per claim 69, 72, 73, 74, Dupree teaches the mechanism of claim 1 wherein the instruction is a YIELD instruction. *(Column 27, lines 55 to 65: The inherent* *instruction issued to access the status of scheduler latch corresponds to the YIELD instruction.)*

As per claim 70, Dupree teaches the mechanism of claim 1 wherein the portion of the record comprises a bit vector. *(Column 25, lines 10 to 20, Column 27, lines 45 to 67: latch and registers all corresponds to bit vector.)*

As per claim 71, Dupree teaches the mechanism of claim 1 wherein the portion of the record comprises one or more multi-bit fields. *(Column 25, lines 10 to 20, Column 27, lines 45 to 67)*

As per claim 78, Dupree teaches the method of claim 76 further comprising suspending the program thread from execution in response to the instruction when the parameter equals a second value, wherein the second value is different from the first value. *(Column 23, lines 1 to 5, Column 25, lines 50 to 67, Column 26, lines 15 to 30: there are different states for a context. The bidding state corresponds to thread suspension. When it is in the bidding state, the context has been scheduled unconditionally, and has an interrupt pending. Each state is represented by different values.)*

As per claim 79, Dupree teaches the method of claim 78 wherein the second value indicates that a condition required for execution of the program thread is unsatisfied. *(Column 23, lines 1 to 5, Column 25, lines 50 to 67, Column 26, lines 15 to*

30: So long as an interrupt is pending, it is an indication that requirements for execution is unsatisfied.)

As per claim 80, Dupree teaches the method of claim 79 wherein the condition is encoded within the parameter as a bit vector or value field. *(Column 25, lines 10 to 20, Column 27, lines 45 to 67: latch and registers all corresponds to bit vector.)*

As per claim 81, Dupree teaches the method of claim 78 further comprising rescheduling the program thread in response to the instruction when the parameter equals a third value, wherein the third value is different from the first and second values. *(Column 23, lines 1 to 5, Column 25, lines 50 to 67, Column 26, lines 15 to 30: The idle state and its information corresponds to the third value.)*

As per claim 83, Dupree teaches the method of claim 81 wherein the third value is an odd value. *(Column 25, lines 10 to 16: the thread to be scheduled must have its scheduling bit set to 1, which is an odd value.)*

As per claim 84, Dupree teaches in a processor enabled to support multiple program threads, a method comprising:

> **executing an instruction that accesses a parameter related to thread scheduling, wherein the instruction is included in a program thread;** *(See claim 15 rejection)*
>
> **suspending the program thread from execution in response to the instruction when the parameter equals a first value.** *(Column 25, lines 10 to 20, Column 26, lines 15 to 30, Column 27, lines 45 to 67: Descheduling*

temporarily only to be rescheduled later corresponds to suspending thread. Moreover, zero in the scheduling latch for descheduling corresponds to first value.)

As per claim 85, Dupree teaches the method of claim 84 further comprising rescheduling the program thread in response to the instruction when the parameter equals a second value, wherein the second value is different from the first value. *(Column 25, lines 10 to 20: bit is set to one for rescheduling.)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 21, 7, 35, 48, 62, 82, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dupree et al (Dupree), Patent No. 5,949,994.

As per claim 21, 7, 35, 48, 62, 82, Dupree teaches all of claim 19. Moreover, he teaches using two different numbers, 1 and 0, to represent the presence of a scheduled event and no event is being scheduled, respectively *(Column 25, lines 10 to 15; Column 27, lines 45 to 67)*. **However, he does not specifically state that wherein the parameter is a two's compliment value of negative 1. It is well known that using two's compliment is a mere way of representing a number. Furthermore, any number can be used in a register to indicate an event. It does not matter if it is negative 1 or 1, as long as it is different from another number used to indicate a different type of event. The applicant fails to demonstrate any unexpected results from the use of negative one that cannot also be achieved with the differing values taught by Dupree.**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MengYao Zhe whose telephone number is 571-272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached on 571-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M.Z.

JOSEPH DEL SOLE
SUPERVISORY PATENT EXAMINER
6/11/07